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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,642	06/26/2003	Vincent J. Zimmer	42P16429	8722

7590 02/15/2006

Cory G. Claassen
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
TREAT, WILLIAM M	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,642	ZIMMER ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-28 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. What constitutes servicing "a legacy type hardware interrupt request ('IRQ') by a processor during a native mode runtime of the processor" and how the legacy type hardware interrupt request ('IRQ') occurred during native mode runtime which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

4. Each of applicants' independent claims recite: "receiving a legacy type hardware interrupt request ('IRQ') by a processor during a native mode runtime of the processor" and "servicing the legacy type hardware interrupt request ('IRQ')" or similar language. In applicants' specification it is stated: "Throughout this specification, several terms of art are used. These terms are to take on their ordinary meaning in the art from which they come, unless specifically defined herein or the context of their use would clearly suggest otherwise. 'Native mode runtime' is defined herein as a higher performance state of a processor than a 'legacy mode runtime' of the processor as defined by a number of bits processed in parallel. ... A 'native type hardware IRQ' is defined herein as a hardware IRQ that is serviced with 32-bit or 64-bit code. A 'legacy type hardware

IRQ' is defined herein as a hardware IRQ that is serviced with 16-bit code. 'Servicing an IRQ' is defined herein as the act of executing designated code in response to an IRQ.

5. However, in applicants' Background section applicants state "during the transition phase from legacy 16-bit technology to native 32/64-bit technology, computers must be backward compatible to encourage OEMs to adopt and fully leverage the newer technologies and to ensure stability of systems running legacy 16-bit and native 32/64-bit technologies. One such compatibility issue exists with incorporating legacy type hardware interrupt requests ('IRQs') with native type hardware IRQs. A legacy type hardware IRQ is a hardware IRQ generated by a hardware entity that executes 16-bit code. A native type hardware IRQ is an IRQ generated by a hardware entity that executes or interacts with 32-bit or 64-bit code (e.g., EFI timer tick). FIG. 1 is a block diagram illustrating how a prior art processing system services legacy type hardware IRQs and native type hardware IRQs. Prior art computing systems have two runtime modes for their processor. During a legacy mode runtime (a.k.a. real mode) of the processor, the processor executes 16-bit code. During a native mode runtime (a.k.a. protected mode) of the processor, the processor executes 32-bit or 64-bit code.

6. If applicants have redefined a legacy type hardware IRQ to merely be a hardware IRQ that is serviced with 16-bit code and not, as in the prior art, a hardware IRQ generated by a processor executing 16-bit code, what is generating the IRQ and how? If as in the prior art the processor is executing 16-bit code, then how is the processor in native mode (i.e., 32-bit or 64-bit execution mode) when it is executing 16-bit code?

Applicants' original disclosure omits any explanation which might resolve these questions.

7. Also, applicants' system for servicing any and all interrupt requests seems to require a global interrupt handler that executes only in native mode runtime (p. 7, last 3 lines). At least, the examiner has not discerned another mode of implementation taught by applicants'. If that is true then it would seem legacy type hardware interrupts could not reasonably be defined "as a hardware IRQ that is serviced with 16-bit code", since it seems to require both 16-bit and 32-bit code to service it. Applicants' disclosure seems internally inconsistent.

8. Finally, in describing what constitutes a global interrupt handler applicants reference a document which is neither U.S. patent nor application. They describe the global interrupt handler as "a native type extensible firmware interface ('EFI') driver compliant with the EFI standard framework (e.g., EFI Specification, version 1.10, December 1, 2002)" (p. 13, lines 19-20) and reference that specification through a hyperlink (http//:developer.intel.com/technology/efi) on page 1 at line 19. The description of what constitutes a global interrupt handler would, in the examiner's judgment, be "essential matter" under 37 CFR 1.57(c). It seems important to a written description which is full, clear, concise and exact so as to provide enablement under 112, 1st as well as making clear applicants' best mode. Also, it is important to the task of describing the invention in terms that particularly point out and distinctly claim applicants' invention under the second paragraph of 35 USC 112. A hyperlink is

certainly not appropriate for essential material nor even non-essential material (37 CFR 1.57(d) and MPEP 608.01).

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: as discussed in paragraphs 3-8, *supra*.

11. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. See paragraphs 3-8, *supra*, for a relevant discussion.

13. Due to applicants' severe 35 USC 112 problems the examiner is unable to determine how one might apply relevant art at this time.

14. The prior art made of record and not applied at this time is considered pertinent to applicant's disclosure.

15. Datta (Patent No. 6,081,890).

16. Pletcher et al. (Patent No. 5,596,755).

17. Crawford et al. (Patent No. 6,385,718).

18. Hoerig et al. (Patent No. 6,272,453).

19. Bhagat (Patent No0. 6,917,997).

20. Jagger (Patent No. 5,701,493).

21. Gephardt et al. (Patent No. 5,721,931).

22. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER